VERSAL Space Reference Design

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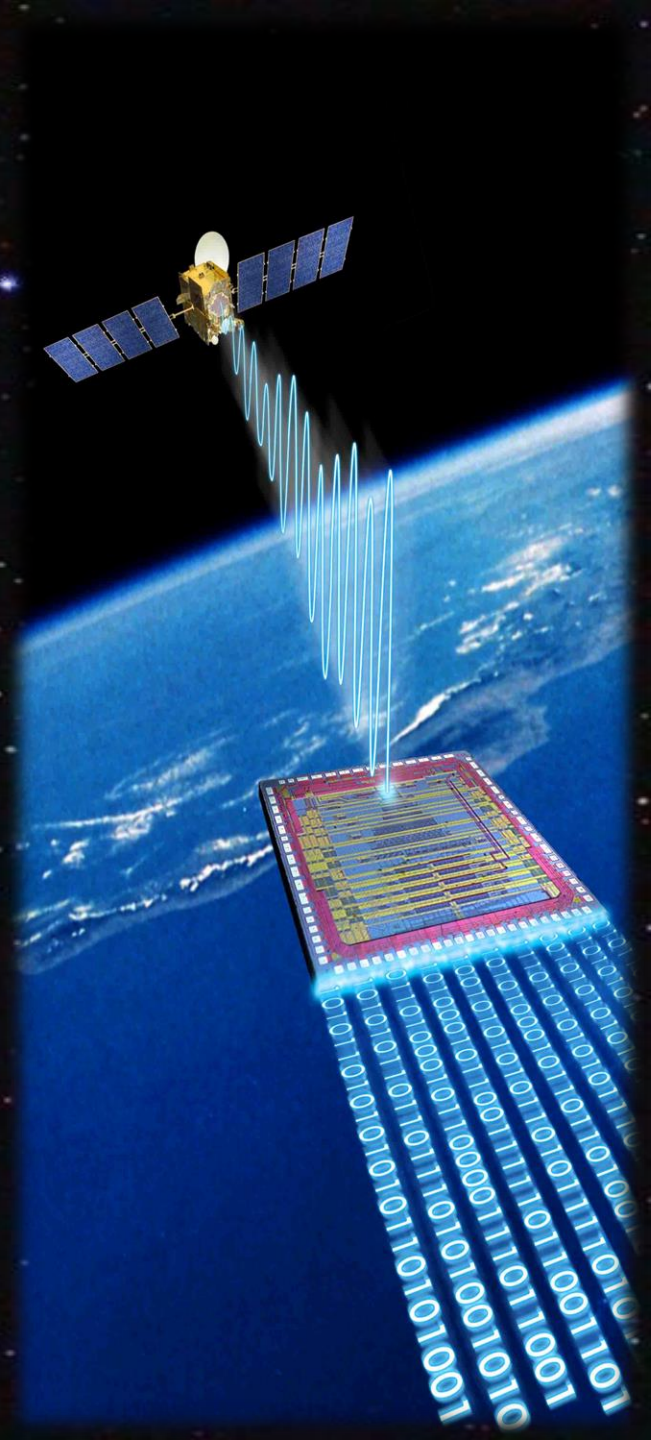
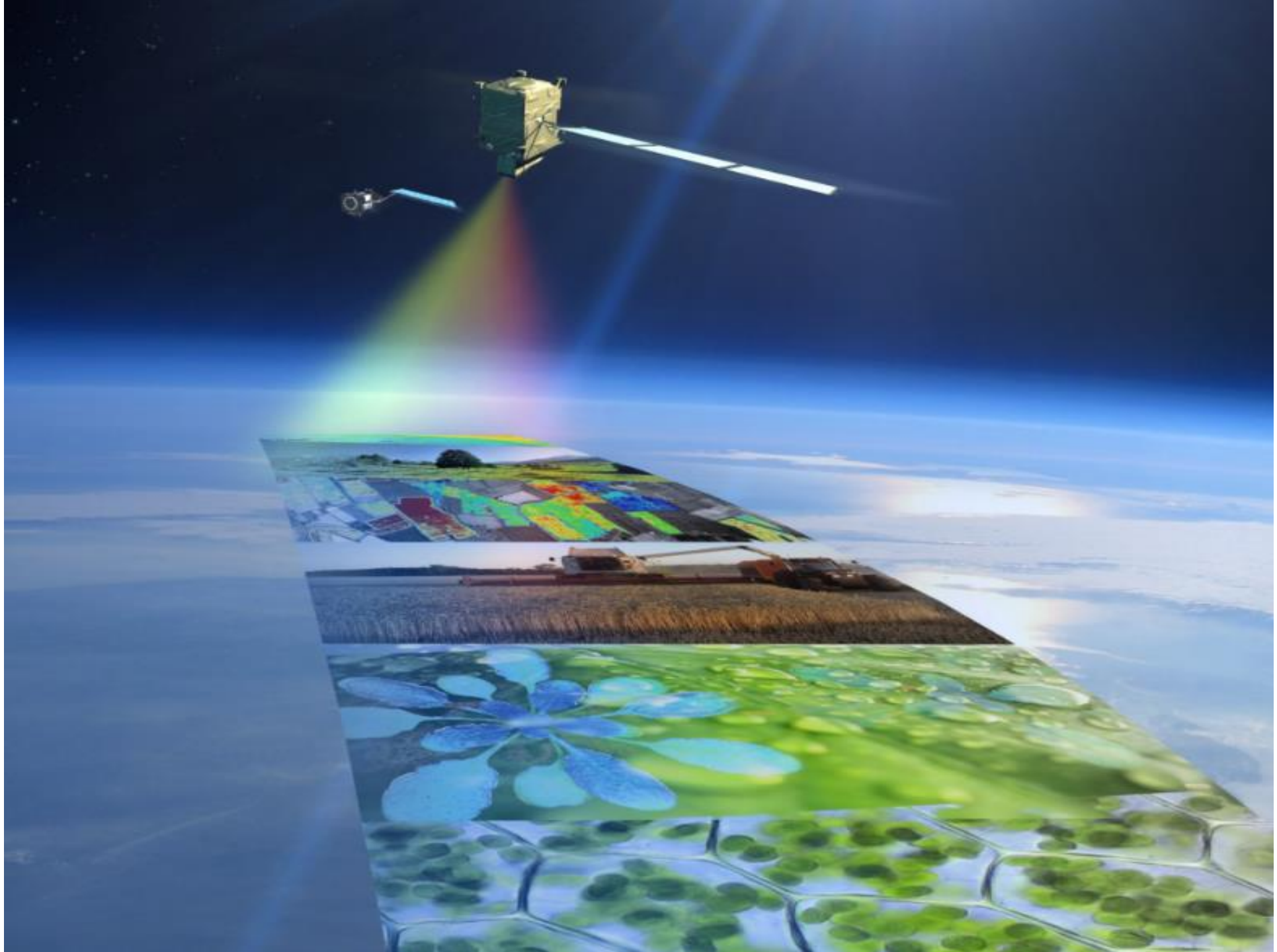
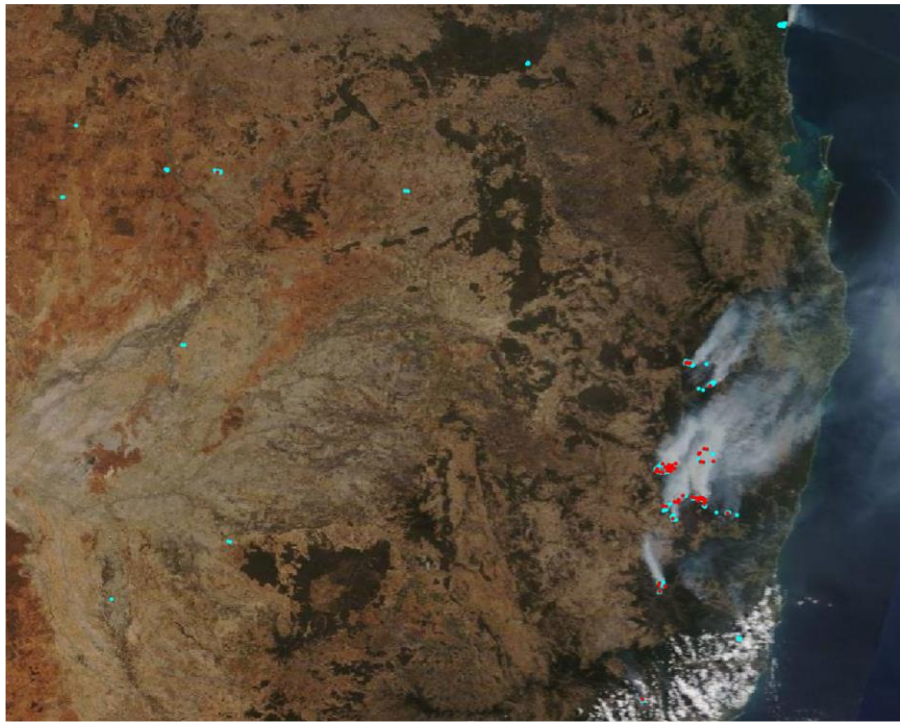


ELEKTRA 2016 WINNER
ELEKTRA 2017 WINNER
ELEKTRA 2018 WINNER

Winner of European Start-Up of 2017 and European High-Reliability Product of 2016, 17 & 18



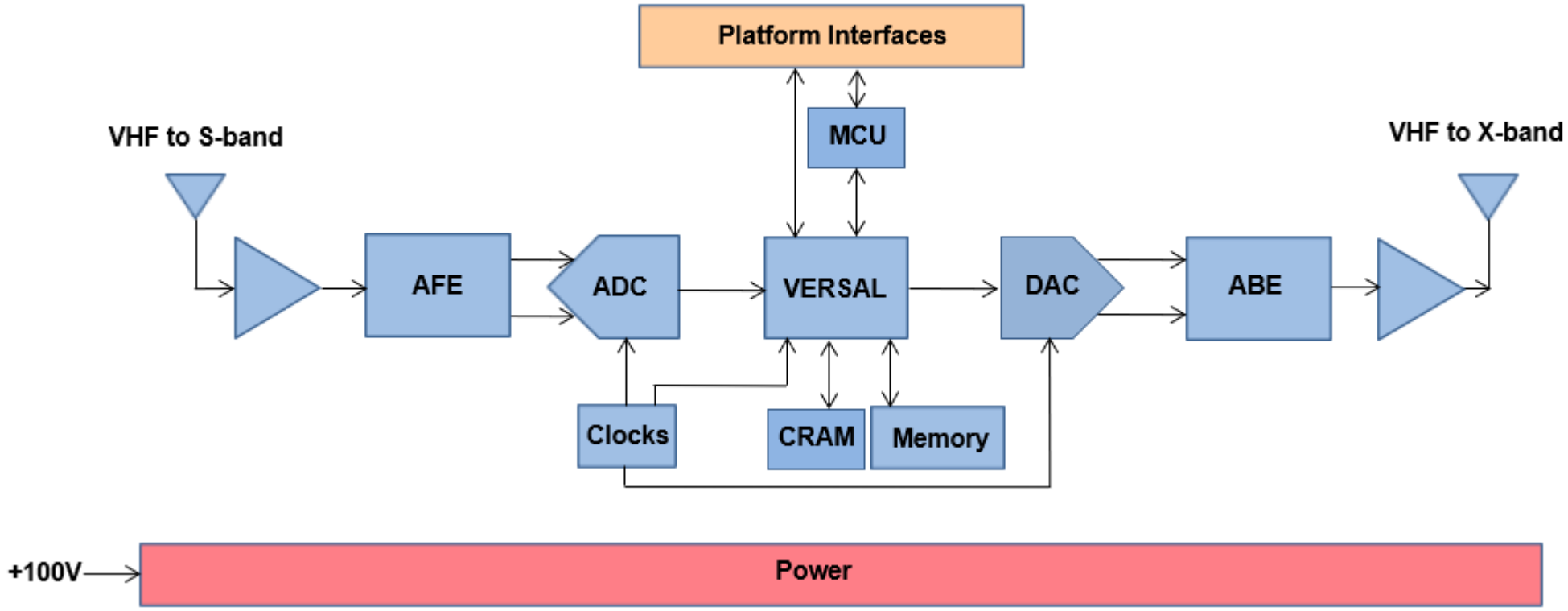
Forest Fire Detection



Space Reference Design Objectives

- *Xilinx's Versal ACAP represents a timely, synergistic and potentially lucrative opportunity to enable in-orbit AI and ML.*
- *Spacechips is bringing to market an EM Versal Space Reference Design (XCVC1902-1MSEVSVA2197) later this year to allow you to prototype and de-risk in-orbit AI and ML. Populated with EM-grade versions of space-grade parts!*
- *Spacechips is bringing to orbit a flight-qualified version next year which you can launch to implement AI and ML in-orbit. Populated with space-qualified components, delivered with EICD, an Instruction Manual and functional HDL to prove operation of the signal-chain blocks – no application code!*

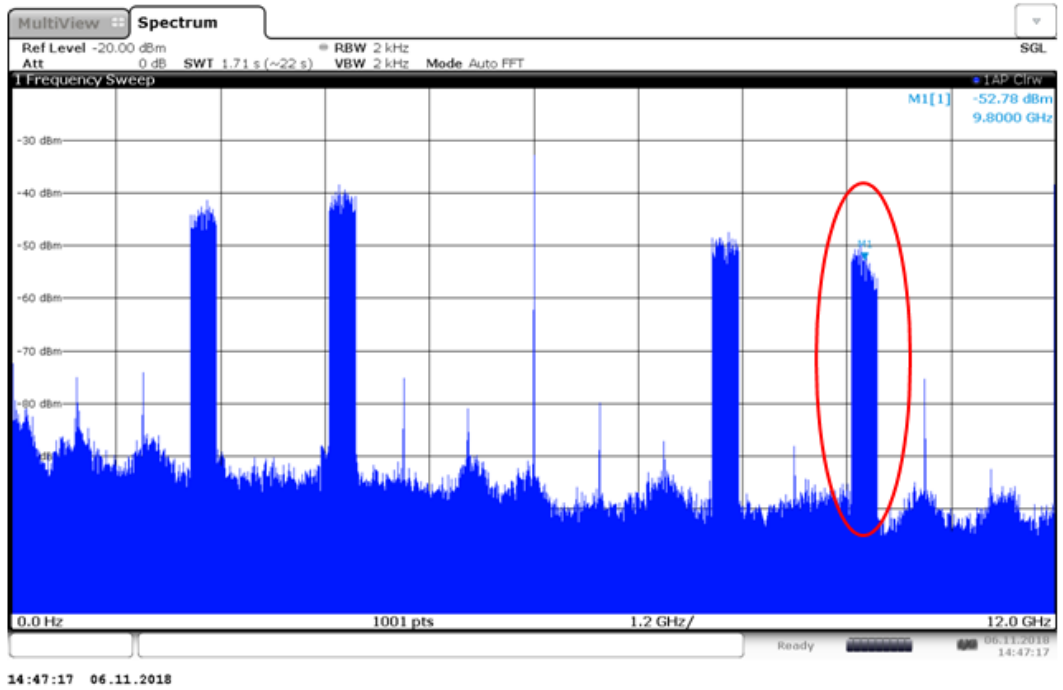
Proposed Architecture

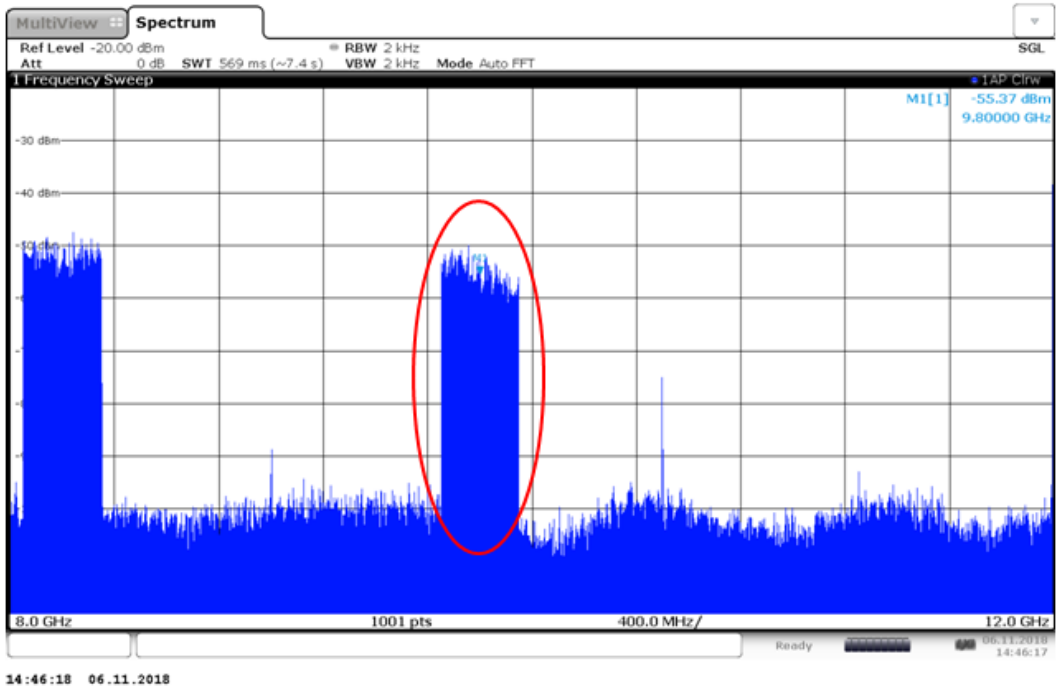


Representative transponder that allows RF traffic to be input, digitised, processed and intelligent analytics extracted in real-time.

Data can be stored using the 1 Tb, non-volatile on-board memory (DDR3-speed) and exported to external sub-systems using a variety of space-industry interfaces such as SpaceWire, SpaceFibre, SPI and CAN.

Direct RF Conversion

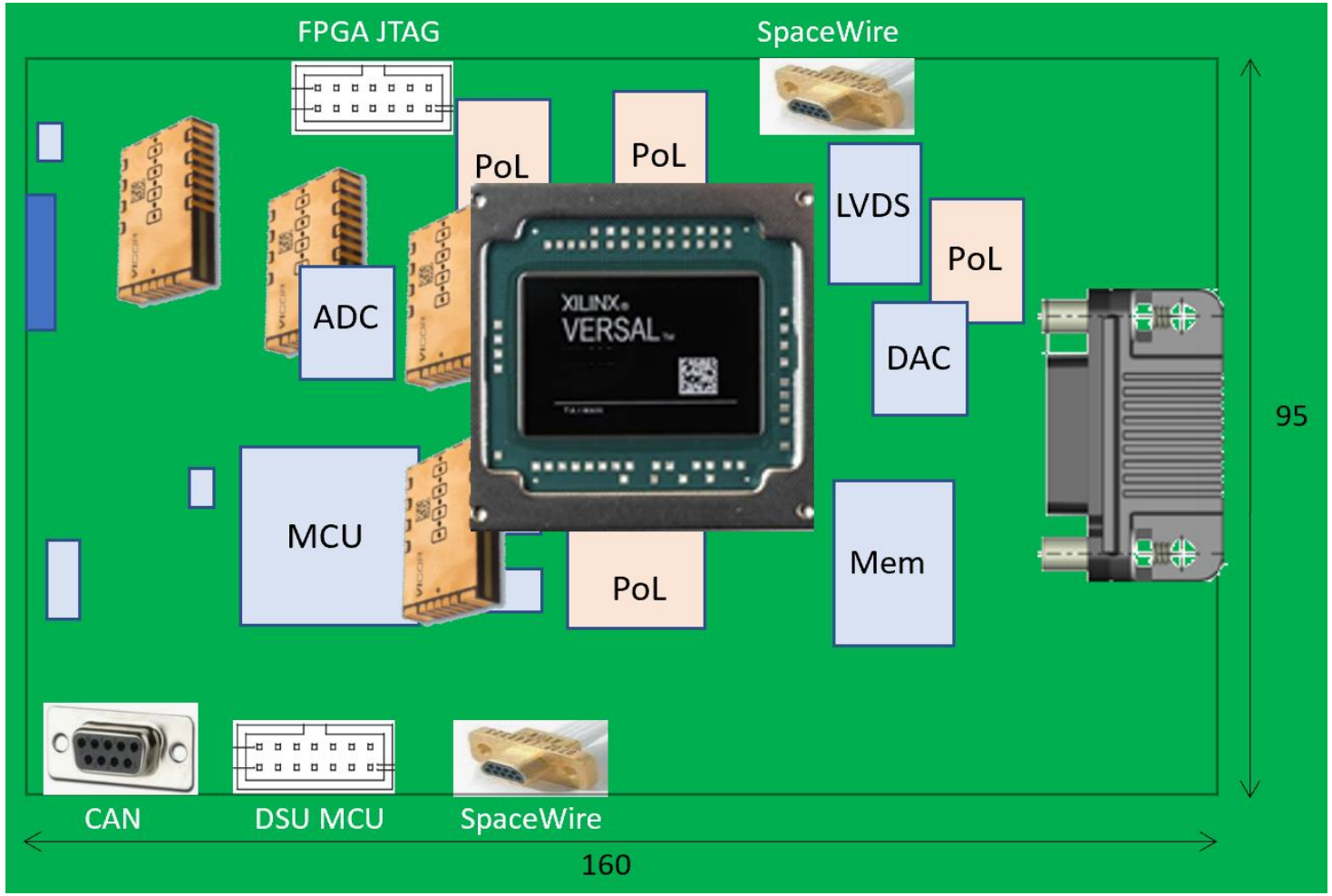




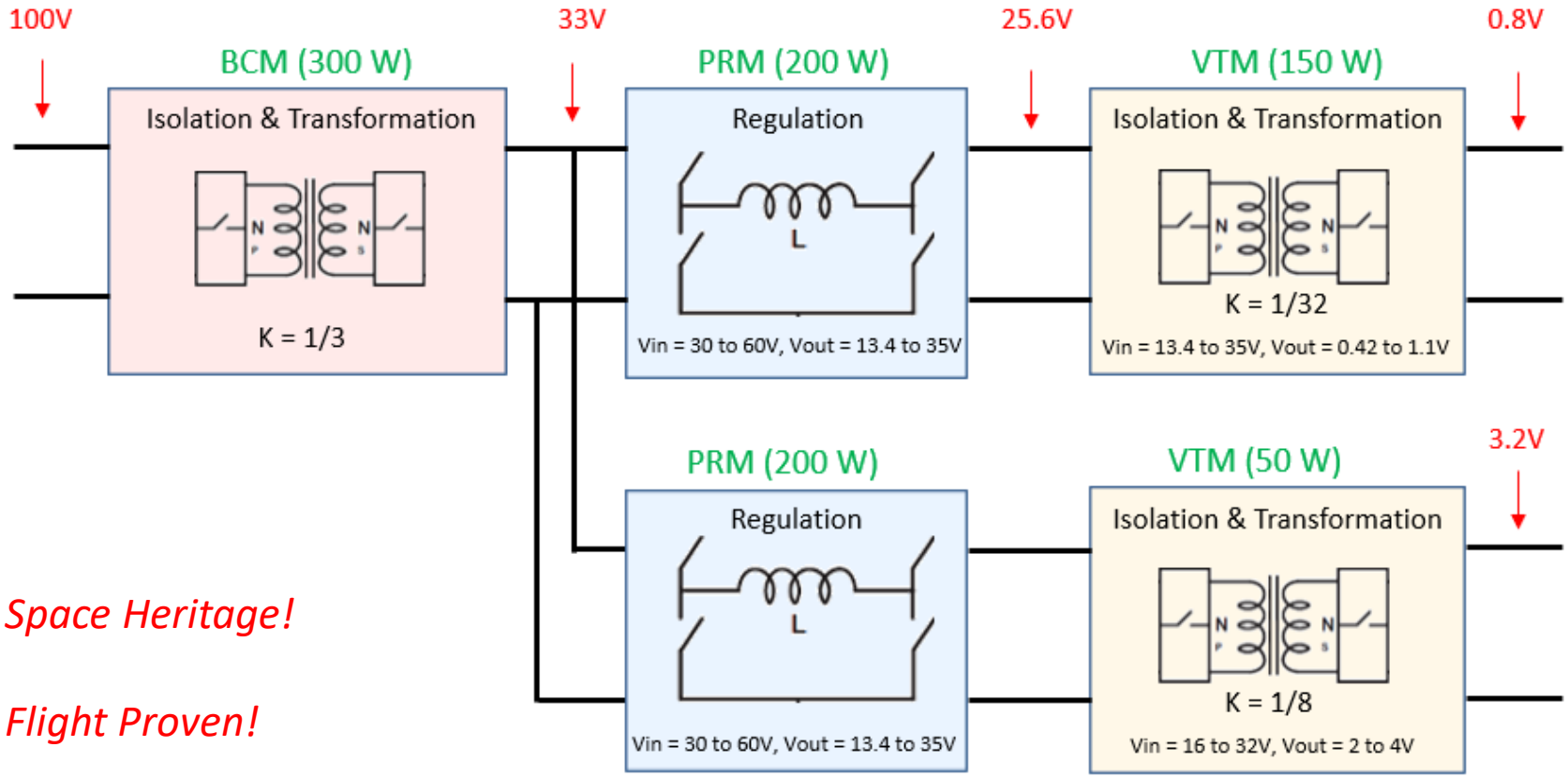
12-bit ADC, Fs = 1.5 GSPS, BW = 3 GHz to digitise up to S-band (Ku/K-band options can also be offered)
12-bit DAC, Fs = 8 GSPS, BW = 7.5 GHz (K-band options can also be offered)

Default build offers fixed sampling rates, options available to allow sampling rate to be changed and re-programmed in-orbit

Implementation 1 : XCVC1902-1MSEVSVA2197



Factorised Power Architecture



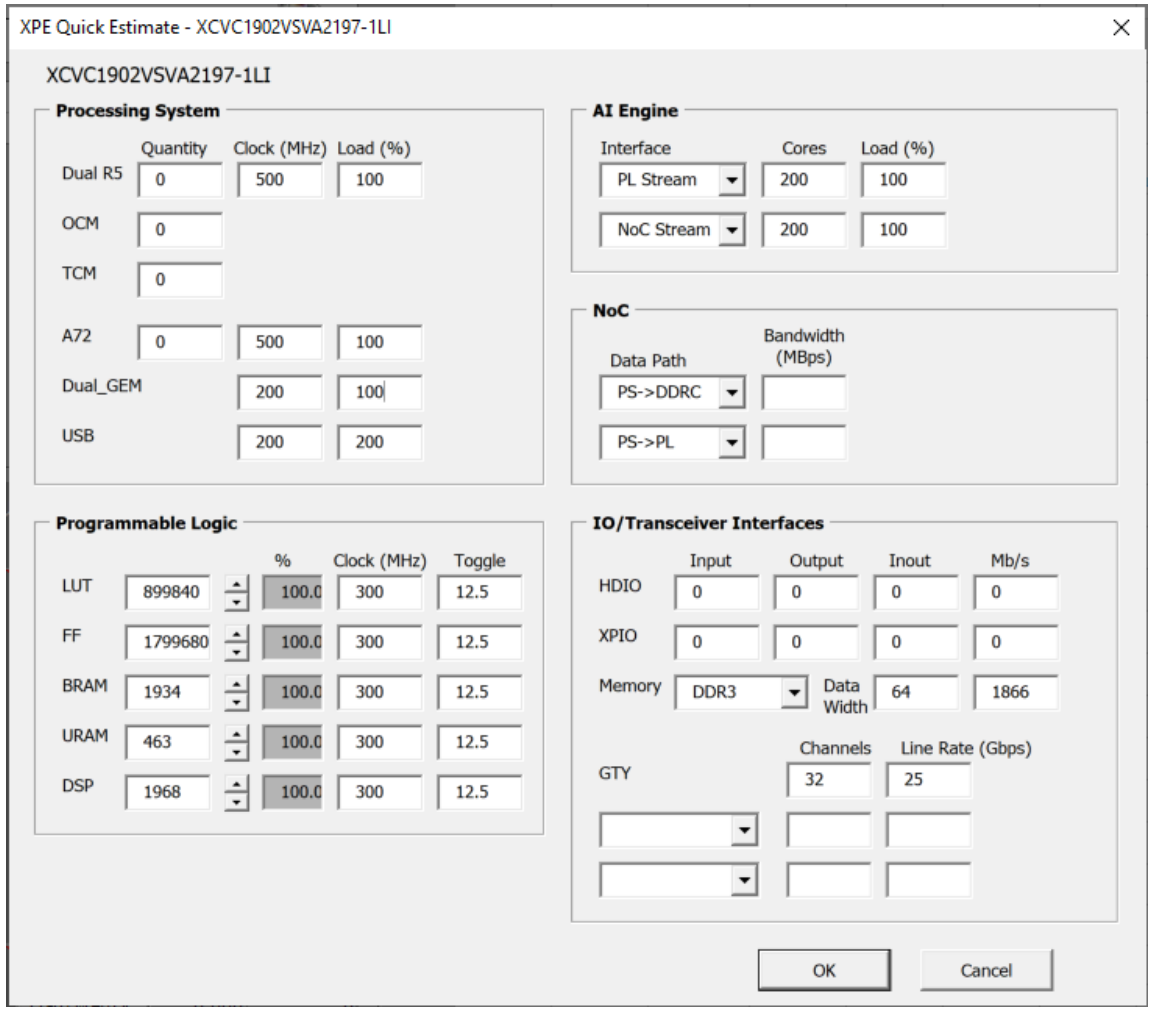
Space Heritage!

Flight Proven!

Versal Power Distribution

Domain/ Sequence no.	Rail Name	Rails	Voltage	DC Spec.	AC Spec.	Current (A)	Power (W)	Step	Comment
LPD/1 PL/1 PMC/1 System/1	PS_IO (Digital)	VCCO_500/1/2/3, VCCO_HDIO, VCCO_XPIO	1.8V – 3.3V (HDIO/PSIO) 1.8V – 3.3V (VCCO_50X) 1V – 1.5V (XPIO)	±1%	±5% (XPIO) (HDIO/PSIO/XPIO)*	0.100 - 3	10	100%	*1.8V, 2.5V at ±5%, and 3.3V at +3/–5% VCCO supplies can be combined if using same Voltage VCCOs must be powered on first in relevant domain
System/2	0V80_SOC _IO (Digital)	VCC_SOC, VCC_IO	0.8V	±1%	±17mV	3.5	3	33%	
PMC/2	0V80_PMC (Digital)	VCC_PMC	0.8V	±1%	±17mV	0.350	0.3	33%	0.88V for PS Overdrive
System/3	1V5_VCCAUX (Digital)	VCCAUX	1.5V	±1%	±2%	4.2	6.3	33%	
LPD/2	0V80_PSLP (Digital)	VCC_PSLP	0.8V	±1%	±17mV	0.300	.2	33%	0.88V for PS Overdrive
FPD/1	0V80_PSFP (Digital)	VCC_PSFP	0.8V	±1%	±17mV	1.5	1.2	70%	0.88V for PS Overdrive
PL/2	0V80_RAM (Digital)	VCCINT, VCC_RAM	0.8V	±1%	±17mV	135	108	33%	200A/us Slew Rate
PMC/3	1V5 (Digital)	VCCAUX_SMON, VCCAUX_PMC	1.5V	±1%	±2%	0.350	.5	100%	
PL/3	0V88 (Analog)	GTAVCC	0.88V	±2%	10mVpp	1.7	1.5	70%	Ripple is steady state, total tolerance is +/-3%. Ripple at FPGA pins, see UG578
PL/4	1V5 (Analog)	GTAVCCAUX	1.5V	±2%	10mVpp	0.100	.2	70%	Ripple is steady state, total tolerance is +/-3%. Ripple at FPGA pins, see UG578
PL/5	1V2 (Analog)	GTAVTT	1.2V	±2%	10mVpp	2.8	3.3	70%	Ripple is steady state, total tolerance is +/-3%. Ripple at FPGA pins, see UG578

XPE Versal Power Distribution

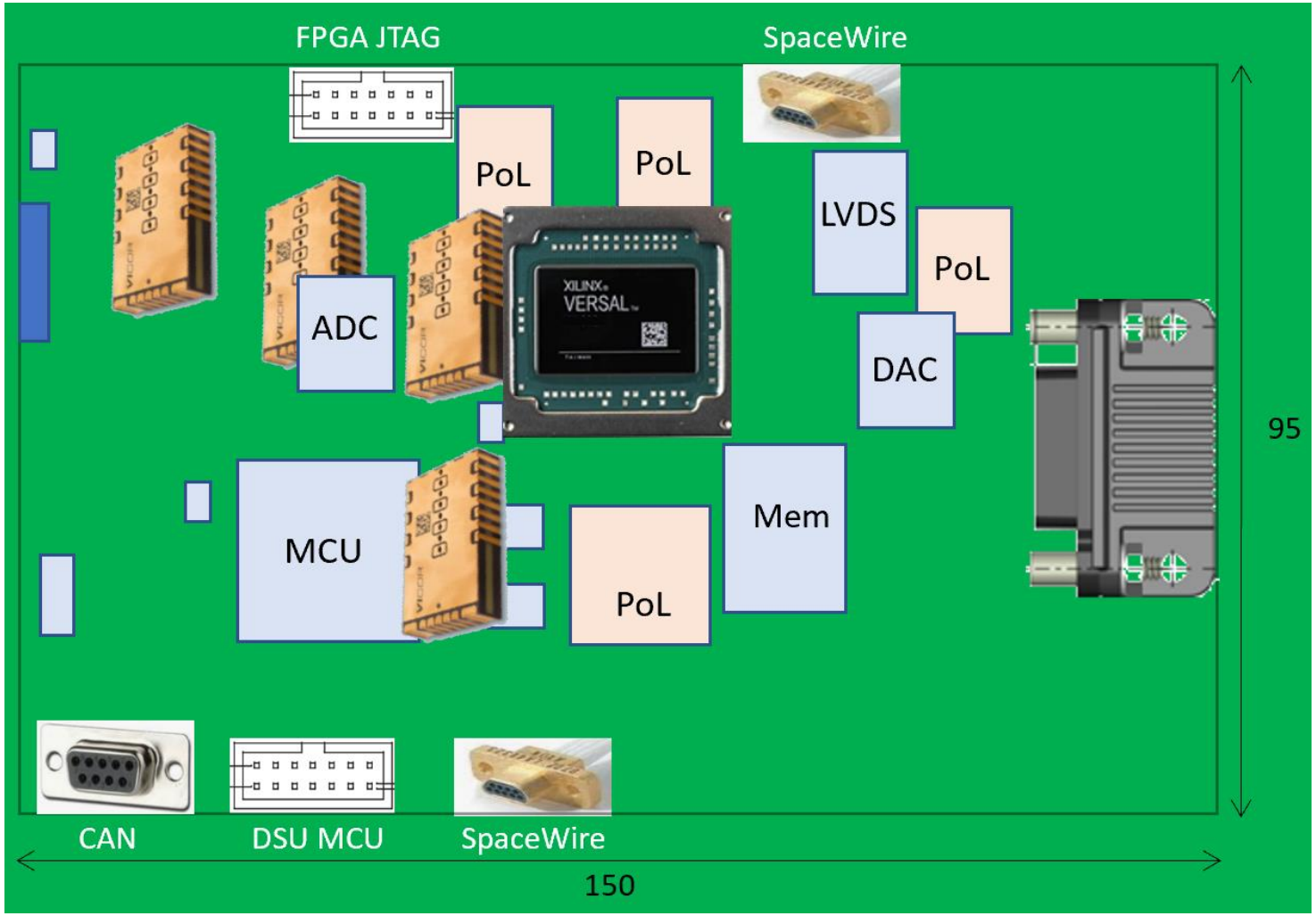


- *When the XCVC1902-1MSEVSVA2197 is fully implemented, its 0.8 V core voltage will draw around 140 A with a total device dissipation of 130 W.*
- *57% of the overall power is consumed by the AI engines*
- *13% by logic*
- *10% by the high-speed transceivers*
- *10% by clocking and PLLs*
- *5% by processors and the remainder by memory and interfaces*

Conclusion

- *Spacechips is bringing to market an EM Versal Space Reference Design (XCVC1902-1MSEVSVA2197) later this year to allow you to prototype and de-risk in-orbit AI and ML.*
    - *Populated with EM-grade versions of space-grade parts and delivered as a tested, populated 2U PCB with or without a housing!*
- *Spacechips will bring to market a flight-qualified version next year which you can launch to implement AI and ML in-orbit. Populated with space-qualified components, delivered as a 2U housed sub-system, with EICD, an Instruction Manual and functional HDL to prove operation of the signal-chain blocks – no application code!*
- *Orders for the XCVC1902-1MSEVSVA2197 EM Versal Space Reference Design currently being taken - includes an EICD, an Instruction Manual and functional HDL to prove operation of the signal-chain blocks – no application code!*
- *In 2024, Spacechips will consider a lower-power EM and FM versions of the Versal Space Reference Design baselining the smaller XCVE2302-1MLISFVA784 ACAP.*

Implementation 2 : XCVE2302-1MLISFVA784



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- *Orders for the XCVC1902-1MSEVSVA2197 EM Versal Space Reference Design currently being taken - includes an EICD, an Instruction Manual and functional HDL to prove operation of the signal-chain blocks – no application code!*

- *Feedback – is there something on the Versal Space Reference Design which is currently missing but you would like to see?*

Space Electronics

Space-Systems Engineering

How to Select & Use COTS Components

PCB Design for Space Applications

Testing Satellite Payloads

Mission Design, Frequency Planning & Link-Budget Analyses

In-Orbit AI and Machine Learning for On-Board Processing

Satellite Applications, Remote Sensing and Geospatial Processing

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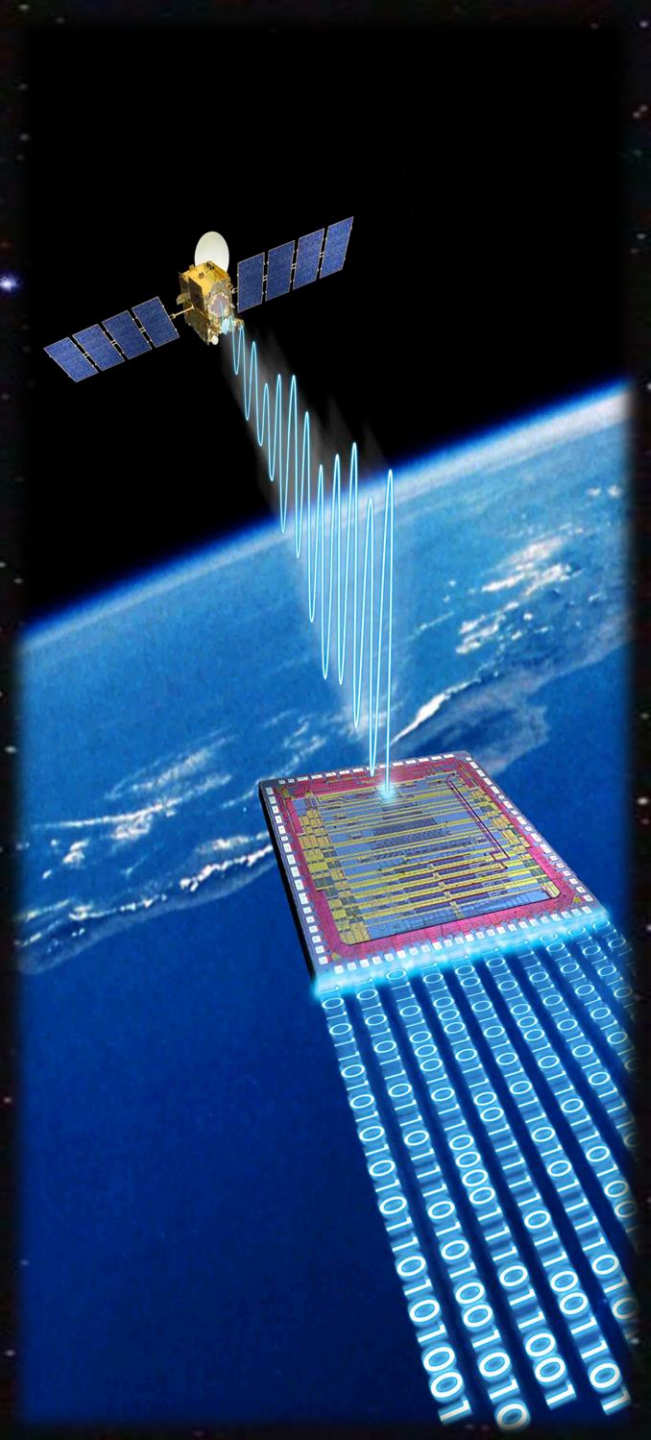

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